Table of Contents

The Authors	xi
Dedications	xiii
Preface	xv
Introduction	xix
Contributing Authors in Order of Appearance	xxi
PART I ANALYZING AND DRIVING VERIFICATION: AN EXECUTIVE'S GUIDE	1
Chapter 1 The Verification Crisis	3
Chapter 2 Automated Metric-Driven Processes Introduction The Process Model The Automated Metric-Driven Process Model Project Management Using Metric-Driven Data What Are Metrics For? Tactical and Strategic Metrics Summary	13 13 15 16 28 29 29 30
Chapter 3 Roles in a Verification Project Introduction The Executive Marketing Design Manager Verification Manager Verification Architect/Methodologist Design/System Architect Verification Engineer Design Engineer Regressions Coordinator Debug Coordinator Summary	31 31 31 33 34 34 35 36 37 38 39 40
Chapter 4 Overview of a Verification Project Introduction Summary	41 41 49

vi Table of Contents

Chapter 5 Verification Technologies	51
Introduction	51
Metric-Driven Process Automation Tools	52
Modeling and Architectural Exploration	58
Assertion-Based Verification	63
Simulation-Based Verification	70
Mixed-Signal Verification	73
Acceleration/Emulation-Based Verification	75
Summary	78
PART II MANAGING THE VERIFICATION	
PROCESS	79
Chapter 6 Verification Planning	81
Introduction	81
Chapter Overview	83
Verification Planning	86
Summary	105
Chapter 7 Capturing Metrics	107
Introduction	107
The Universal Metrics Methodology	109
Chapter 8 Regression Management	113
Introduction	113
Early Regression Management Tasks	114
Regression Management	114
Linking the Regression and Revision Management Systems	115
Bring-Up Regressions	116
Integration Regressions	119
Design Quality Regressions	121
Managing Regression Resources and Engineering	
Effectiveness	122
Regression-Centric Metrics	123
How Many Metrics Are Too Many?	125
Summary	127
Chapter 9 Revision Control and Change Integration	129
Introduction	129
The Benefits of Revision Control	131
Metric-Driven Revision Control	132
Summary	139
Chapter 10 Debug	141
Introduction	141

Table of Contents	vii

Debug Metrics Summary	144 153
PART III EXECUTING THE VERIFICATION PROCES	SS 155
Chapter 11 Coverage Metrics	157
Introduction	157
Chapter 12 Modeling and Architectural Verification	163
Introduction	163
How to Plan	164
Tracking to Closure	165
Reusing Architectural Verification Environments	165
Summary	166
Chapter 13 Assertion-Based Verification	167
Introduction	167
How to Plan	170
Tracking to Closure	175
Opportunities for Reuse	177
Summary	179
Chapter 14 Dynamic Simulation-Based Verification	181
Introduction	181
How to Plan	183
Taxonomy of Simulation-Based Verification	187
Tracking to Closure	191
Summary	196
Chapter 15 System Verification	197
Introduction	197
Coverification Defined	199
Advancing SoC Verification	201
List of Challenges	202
ARM926 PrimeXsys Platform Design	205
Closing the Gap	207
DMA Diagnostic Program	208
Connecting the DMA Diagnostic to the Verification Environment	212
Connecting the Main() Function in C	215
Writing Stubs	216
Creating Sequences and Coverage	217
Conclusion	219
References	220

viii Table of Contents

4.1	221
Abstract	222
Introduction	222
Traditional Mixed-Signal Verification	223
Verification Planning	225
Analog Mixed-Signal Verification Kit	229
Conclusion	233
Reference	234
Chapter 17 Design for Test	235
Introduction	236
Motivation	238
A Unified DFT Verification Methodology	239
Planning	240
Executing	241
Automating	243
Test Case	245
Benefits	248
Future Work	249
Conclusions	249
References	250
PART IV CASE STUDIES AND COMMENTARIES Metric-Driven Design Verification: Why Is My Customer a Better	253
Verification Engineer Than Me?	255
A hetract	
Abstract Introduction	255 256
Introduction	256
Introduction Section 1: The Elusive Intended Functionality	256 257
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule	256 257 265
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan	256 257 265 270
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule	256 257 265
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion	256 257 265 270 274
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex	256 257 265 270 274 277
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex Network Processor	256 257 265 270 274 277
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex Network Processor The Task Looked to be Complex	256 257 265 270 274 277 279 280
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex Network Processor The Task Looked to be Complex Discovering Project Predictability	256 257 265 270 274 277 279 280 281
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex Network Processor The Task Looked to be Complex Discovering Project Predictability A Coverage-Driven Approach, a Metric-Driven Environment	256 257 265 270 274 277 279 280 281 282
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex Network Processor The Task Looked to be Complex Discovering Project Predictability	256 257 265 270 274 277 279 280 281
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex Network Processor The Task Looked to be Complex Discovering Project Predictability A Coverage-Driven Approach, a Metric-Driven Environment	256 257 265 270 274 277 279 280 281 282
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex Network Processor The Task Looked to be Complex Discovering Project Predictability A Coverage-Driven Approach, a Metric-Driven Environment A New Level of Confidence Developing a Coverage-Driven SoC Methodology Introduction	256 257 265 270 274 277 279 280 281 282 283
Introduction Section 1: The Elusive Intended Functionality Section 2: The Ever-Shrinking Schedule Section 3: Writing a Metric-Driven Verification Plan Section 4: Implementing the Metric-Driven Verification Plan Conclusion Metric-Driven Methodology Speeds the Verification of a Complex Network Processor The Task Looked to be Complex Discovering Project Predictability A Coverage-Driven Approach, a Metric-Driven Environment A New Level of Confidence Developing a Coverage-Driven SoC Methodology	256 257 265 270 274 277 279 280 281 282 283

Tabl	le of C	Contents	ix
I ao	ic or c	Contents	1/1

Coverage and Checking	292
Results and Futures	293
From Panic-Driven to Plan-Driven Verification Managing	
the Transition	297
Verification of a Next-Generation Single-Chip Analog TV	
and Digital TV ASIC	303
Abstract	303
Introduction	304
The Design	305
Verification Challenges	306
Addition of New Internal Buses	307
Module-Level Verification	309
Data Paths and Integration Verification	309
Management of Verification Process and Data	309
Key Enablers of the Solution	310
Results	320
Conclusions	322
Future Work	322
Management IP: New Frontier Providing Value Enterprise-Wide	325
Adelante VD3204x Core, SubSystem, and SoC Verification	329
Abstract	330
Introduction	330
Project Background	331
Verification Decisions	333
DSP Core Verification	335
DSP Subsystem Verification	338
SoC-Level Verification	341
Results and Future Work	342
SystemC-based Virtual SoC: An Integrated System-Level	
and Block-Level Verification Approach from Simulation to Coemulation	345
Abstract	345 346
Introduction: Verification and Validation Challenges	340
Virtual SoC TLM Platform	348
Functional Verification: Cosimulation TLM and RTL	350
Validation: Coemulation TLM-Palladium	352
Conclusion and Future Developments	353
Is Your System-Level Project Benefiting from Collaboration	
or Headed to Chaos?	355
Index	359