Preface xv
From the Old to the New xvii
Acknowledgments xxi

1 Verilog – A Tutorial Introduction 1

Getting Started 2
A Structural Description 2
Simulating the binaryToESeg Driver 4
Creating Ports For the Module 7
Creating a Testbench For a Module 8
Behavioral Modeling of Combinational Circuits 11
Procedural Models 12
Rules for Synthesizing Combinational Circuits 13
Procedural Modeling of Clocked Sequential Circuits 14
Modeling Finite State Machines 15
Rules for Synthesizing Sequential Systems 18
Non-Blocking Assignment ("<=") 19
Module Hierarchy 21
The Counter 21
A Clock for the System 21
Tying the Whole Circuit Together 22
Tying Behavioral and Structural Models Together 25
Summary 27
Exercises 28

2 Logic Synthesis 35

Overview of Synthesis 35
Register-Transfer Level Systems 35
Disclaimer 36
Combinational Logic Using Gates and Continuous Assign 37
Procedural Statements to Specify Combinational Logic 40
The Basics 40

Complications — Inferred Latches 42
Using Case Statements 43
Specifying Don't Care Situations 44
Procedural Loop Constructs 46
Inferring Sequential Elements 48
Latch Inferences 48
Flip Flop Inferences 50
Summary 52
Inferring Tri-State Devices 52
Describing Finite State Machines 53
An Example of a Finite State Machine 53
An Alternate Approach to FSM Specification 56
Finite State Machine and Datapath 58
A Simple Computation 58
A Datapath For Our System 58
Details of the Functional Datapath Modules 60
Wiring the Datapath Together 61
Specifying the FSM 63
Summary on Logic Synthesis 66
Exercises 68

3 **Behavioral Modeling** 73

Process Model 73
If-Then-Else 75
Where Does The ELSE Belong? 80
The Conditional Operator 81
Loops 82
Four Basic Loop Statements 82
Exiting Loops on Exceptional Conditions 85
Multi-way Branching 86
If-Else-If 86
Case 86
Comparison of Case and If-Else-If 89
Casez and Casex 90
Functions and Tasks 91
Tasks 93
Functions 97
A Structural View 100
Rules of Scope and Hierarchical Names 102
Rules of Scope 102
Hierarchical Names 105

Summary 106
Exercises 106

4 Concurrent Processes 109

Concurrent Processes 109
Events 111
Event Control Statement 112
Named Events 113
The Wait Statement 116
A Complete Producer-Consumer Handshake 117
Comparison of the Wait and While Statements 120
Comparison of Wait and Event Control Statements 121
A Concurrent Process Example 122
A Simple Pipelined Processor 128
The Basic Processor 128
Synchronization Between Pipestages 130
Disabling Named Blocks 132
Intra-Assignment Control and Timing Events 134
Procedural Continuous Assignment 136
Sequential and Parallel Blocks 138
Exercises 140

5 Module Hierarchy 143

Module Instantiation and Port Specifications 143
Parameters 146
Arrays of Instances 150
Generate Blocks 151
Exercises 154

6 Logic Level Modeling 157

Introduction 157
Logic Gates and Nets 158
Modeling Using Primitive Logic Gates 159
Four-Level Logic Values 162
Nets 163
A Logic Level Example 166
Continuous Assignment 171
Behavioral Modeling of Combinational Circuits 172
Net and Continuous Assign Declarations 174
A Mixed Behavioral/Structural Example 176
Logic Delay Modeling 180
A Gate Level Modeling Example 181
Gate and Net Delays 182
Specifying Time Units 185
Minimum, Typical, and Maximum Delays 186
Delay Paths Across a Module 187
Summary of Assignment Statements 189
Summary 190
Exercises 191

7 Cycle-Accurate Specification 195

Cycle-Accurate Behavioral Descriptions 195
Specification Approach 195
A Few Notes 197
Cycle-Accurate Specification 198
Inputs and Outputs of an Always Block 198
Input/Output Relationships of an Always Block 199
Specifying the Reset Function 202
Mealy/Moore Machine Specifications 203
A Complex Control Specification 204
Data and Control Path Trade-offs 204
Introduction to Behavioral Synthesis 209
Summary 210

8 Advanced Timing 211

Verilog Timing Models 211
Basic Model of a Simulator 214
Gate Level Simulation 215
Towards a More General Model 215
Scheduling Behavioral Models 218
Non-Deterministic Behavior of the Simulation Algorithm 220
Near a Black Hole 221
It's a Concurrent Language 223
Non-Blocking Procedural Assignments 226
Contrasting Blocking and Non-Blocking Assignments 226
Prevalent Usage of the Non-Blocking Assignment 227
Extending the Event-Driven Scheduling Algorithm 228
Illustrating Non-Blocking Assignments 231
Summary 233
Exercises 234

9 User-Defined Primitives 239

Combinational Primitives 240
Basic Features of User-Defined Primitives 240
Describing Combinational Logic Circuits 242
Sequential Primitives 243
Level-Sensitive Primitives 244
Edge-Sensitive Primitives 244
Shorthand Notation 246
Mixed Level- and Edge-Sensitive Primitives 246
Summary 249
Exercises 249

10 Switch Level Modeling 251

A Dynamic MOS Shift Register Example 251
Switch Level Modeling 256
Strength Modeling 256
Strength Definitions 259
An Example Using Strengths 260
Resistive MOS Gates 262
Ambiguous Strengths 263
Illustrations of Ambiguous Strengths 264
The Underlying Calculations 265
The miniSim Example 270
Overview 270
The miniSim Source 271
Simulation Results 280
Summary 281
Exercises 281

11 Projects 283

Modeling Power Dissipation 283
Modeling Power Dissipation 284
What to do 284
Steps 285
A Floppy Disk Controller 286
Introduction 286
Disk Format 287
Function Descriptions 288
Reality Sets In... 291
Everything You Always Wanted to Know about CRC's 291
Supporting Verilog Modules 292

Appendix A: Tutorial Questions and Discussion 293
Structural Descriptions 293
Testbench Modules 303
Combinational Circuits Using always 303

Sequential Circuits 305
Hierarchical Descriptions 308

Appendix B: Lexical Conventions 309
White Space and Comments 309
Operators 310
Numbers 310
Strings 311
Identifiers, System Names, and Keywords 312

Appendix C: Verilog Operators 315
Table of Operators 315
Operator Precedence 320
Operator Truth Tables 321
Expression Bit Lengths 322

Appendix D: Verilog Gate Types 323
Logic Gates 323
BUF and NOT Gates 325
BUFIF and NOTIF Gates 326
MOS Gates 327
Bidirectional Gates 328
CMOS Gates 328
Pullup and Pulldown Gates 328

Appendix E: Registers, Memories, Integers, and Time 329
Registers 329
Memories 330
Integers and Times 331

Appendix F: System Tasks and Functions 333
Display and Write Tasks 333
Continuous Monitoring 334
Strobed Monitoring 335
File Output 335
Simulation Time 336
Stop and Finish 336
Random 336
Reading Data From Disk Files 337

Appendix G: Formal Syntax Definition 339
Tutorial Guide to Formal Syntax Specification 339

Source text 343
Declarations 346
Primitive instances 351
Module and generated instantiation 353
UDP declaration and instantiation 355
Behavioral statements 355
Specify section 359
Expressions 365
General 370
Index 373